What is claimed is:

1. A system for designing connecting terminals of a semiconductor device, comprising:

a power supply cell arranging unit configured to arrange power supply cells at some of I/O slots formed in a semiconductor chip;

an I/O signal cell arranging unit configured to arrange I/O signal cells at some of the I/O slots where the power supply cells are not arranged;

a first connecting net generator configured to generate a first connecting net connecting the I/O slots to bumps formed on the semiconductor chip;

a second connecting net generator configured to generate a second connecting net connecting the bumps to external electrodes formed on a package base; and

a verifier configured to verify whether the power supply cells, I/O signal cells, and first and second connecting nets violate predetermined design rules.

2. The system of claim 1, wherein the first connecting net connects the I/O slots where the power supply cells and I/O signal cells are arranged to the bumps, and the second connecting net connects the bumps that are connected to the I/O slots through the first connecting net to the external electrodes.

3. The system of claim 1, wherein the bumps are formed over a principle surface of the semiconductor chip, and the external electrodes are formed over a principle surface of the package base.

4. The system of claim 1, wherein the design rules include:

a power supply cell arranging rule concerning the number and locations of the power supply cells;

an I/O signal cell arranging rule concerning the sizes of the I/O signal cells and prohibited areas where the I/O signal cells must not be arranged; and

a connecting pin arranging rule concerning requirements for equal-length wires and pair wires, a restriction on the number of intersections in each of the first and second connecting nets, and a maximum wiring length.

5. The system of claim 1, wherein the power supply cell arranging unit arranges the power supply cells according to a power supply cell arranging rule concerning the number and locations of the power supply cells, the I/O signal cell arranging unit arranges the I/O signal cells according to an I/O signal cell arranging rule concerning the sizes of the I/O signal cells and prohibited areas where

the I/O signal cells must not be arranged, and the first and second connecting net generators generate the first and second connecting nets according to a connecting pin arranging rule concerning requirements for equal-length wires and pair wires, a restriction on the number of intersections in each of the first and second connecting nets, and a maximum wiring length.

6. A method of designing connecting terminals of a semiconductor device, comprising:

arranging power supply cells at some of I/O slots formed in a semiconductor chip;

arranging I/O signal cells at some of the I/O slots where the power supply cells are not arranged;

generating a first connecting net connecting the I/O slots to bumps formed on the semiconductor chip;

generating a second connecting net connecting the bumps to external electrodes formed on a package base; and

verifying whether the power supply cells, I/O signal cells, and first and second connecting nets violate predetermined design rules.

7. The method of claim 6, wherein the first connecting net is generated after arranging the power supply cells and I/O signal cells, and the second connecting net is

generated after generating the first connecting net.

8. The method of claim 6, wherein the design rules include:

a power supply cell arranging rule concerning the number and locations of the power supply cells;

an I/O signal cell arranging rule concerning the sizes of the I/O signal cells and prohibited areas where the I/O signal cells must not be arranged; and

a connecting pin arranging rule concerning requirements for equal-length wires and pair wires, a restriction on the number of intersections in each of the first and second connecting nets, and a maximum wiring length.

9. The method of claim 6, wherein the power supply cells are arranged according to a power supply cell arranging rule concerning the number and locations of the power supply cells, the I/O signal cells are arranged according to an I/O signal cell arranging rule concerning the sizes of the I/O signal cells and prohibited areas where the I/O signal cells must not be arranged, and the first and second connecting nets are arranged according to a connecting pin arranging rule concerning requirements for equal-length wires and pair wires, a restriction on the number of intersections in each of the first and second connecting

nets, and a maximum wiring length.

10. A computer program product for designing connecting terminals of a semiconductor device, comprising:

instructions configured to arrange power supply cells at some of I/O slots formed in a semiconductor chip;

instructions configured to arrange I/O signal cells at some of the I/O slots where the power supply cells are not arranged;

instructions configured to generate a first connecting net connecting the I/O slots to bumps formed on the semiconductor chip;

instructions configured to generate a second connecting net connecting the bumps to external electrodes formed on a package base; and

instructions configured to verify whether the power supply cells, I/O signal cells, and first and second connecting nets violate predetermined design rules.

11. The computer program product of claim 10, wherein the first connecting net is generated after arranging the power supply cells and I/O signal cells, and the second connecting net is generated after generating the first connecting net.

12. The computer program product of claim 10, wherein

the design rules include:

a power supply cell arranging rule concerning the number and locations of the power supply cells;

an I/O signal cell arranging rule concerning the sizes of the I/O signal cells and prohibited areas where the I/O signal cells must not be arranged; and

a connecting pin arranging rule concerning requirements for equal-length wires and pair wires, a restriction on the number of intersections in each of the first and second connecting nets, and a maximum wiring length.

13. The computer program product of claim 10, wherein the power supply cells are arranged according to a power supply cell arranging rule concerning the number and locations of the power supply cells, the I/O signal cells are arranged according to an I/O signal cell arranging rule concerning the sizes of the I/O signal cells and prohibited areas where the I/O signal cells must not be arranged, and the first and second connecting nets are arranged according to a connecting pin arranging rule concerning requirements for equal-length wires and pair wires, a restriction on the number of intersections in each of the first and second connecting nets, and a maximum wiring length.